ITRI
ERSO

ES15494

ADVANCED CLOCK GENERATOR

FEATURES:

- Guaranteed performance up to 140MHz
- 16 video clock rates and 8 memory clock rates
- Glitch-free clock frequency transition
- Mask-programmable frequencies
- Internal Clock remains locked when the external frequency input is selected
- Low power sub-μ CMOS technology
- Buffered crystal oscillator clock output
- Built-in loop filter

APPLICATIONS:

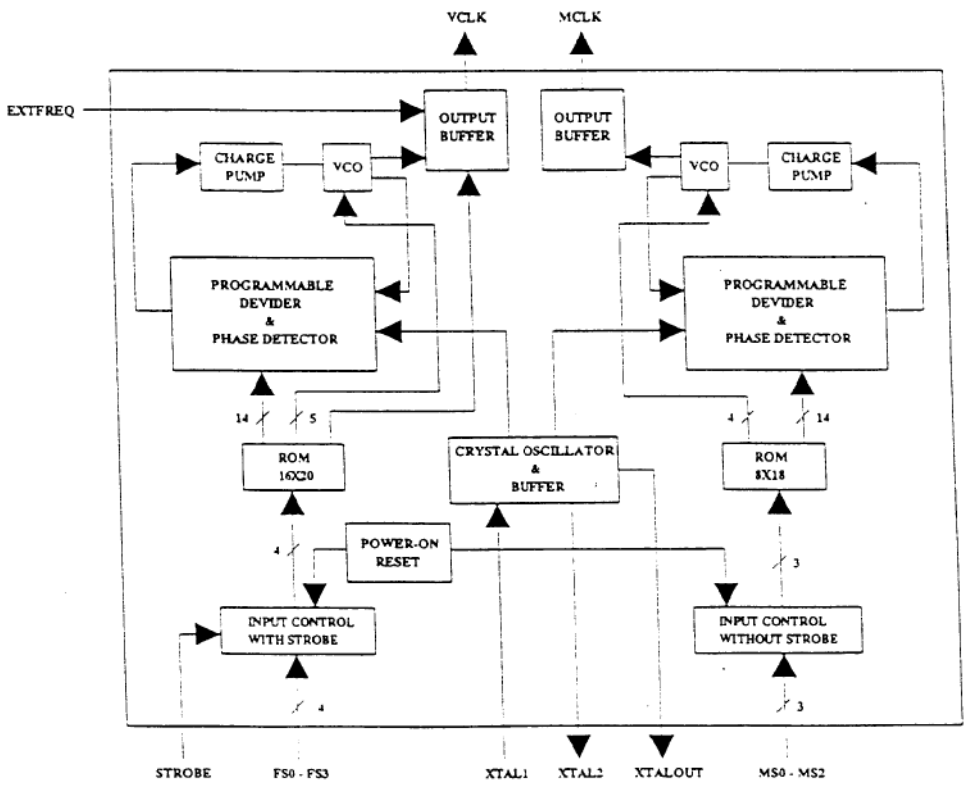
- VGA, super VGA video addapters
- Workstations
- 8514A, TMS34010, TMS34020
- Motherboard

GENERAL DESCRIPTION:

The dual video/memory clock generator is a PLL frequency synthesizer which can generate 16 video clock frequencies and & memory clock frequencies for video display systems. The outputs are designed to be compatible with MDA, CGA, MCGA, EGA, VGA, XGA as well as the higher frequencies needed for advanced applications in workstation graphics. In addition to providing 16 video clock rates. The external generated signal can be multiplexd to the video clock output (VCLK). The crystal oscillator signal can be used to provide the bus lock for the rest of the system through XTALOUT output.

When the modes are selected, the internal phase locked frequencies continue to remain at their preset values. This feature allows internal clock to remain locked when the external frequency input is selected. For the reason of low power and low cost. It is necessary to implement all analog, digital and memory functions by CMOS technology.

FUNCTION BLOCK DLAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC supply voltage	V_{DD}	-0.5~7	V
Digital input voltage	V_{IN}	-0.5~V_{DD}+0.5	V
Operating temperature	T_A	0~70	℃
Storage temperature	T_{stag}	-65~125	℃
Power dissipation	Po	500	MW

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Funcitional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating condition periods may affect device reliability.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage range	V_{DD}	4	5	5.5	V	
Input low voltage	V_{IL}	V_{SS}	-	0.8		V_{DD} =5V
Input high voltage	V_{IH}	2	-	V_{DD}		V_{DD} =5V
Inpt leakage current	V_{IN}	-	-	10		
Output low voltage	I_{OL}	-	-	0.4		I_O = 4mA
Output high voltage	V_{OH}	2.4	-	-		I_O = 4mA
Operating current	I_{DD}	-	-	27		VCLK = 80MHz,MCLK = 50MHz
Input pin capacitance	C_{IN}	-	-	8		f = 1MHz
Output pin capacitance	C_{OUT}	-	-	12		f = 1MHz

AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Condition
Strobe pulse width	T_W	20	-	ns	Xtal = 14.318MHz
Setup time	T_{SU}	10	-	ns	C_{LOAD} = 25Pf
Hold time	T_H	10	-	ns	T = 25℃
VCLK, MCLK					Duty cycle measured
Rise time	T_R	-	2	ns	At 1.4V:40%~60%
Fall time	T_F	-	2	ns	
Frequency error	-	-	0.5	%	T_R and T_F measured
Maximum frequency	-	-	140	MHz	between 0.8V & 2.0V

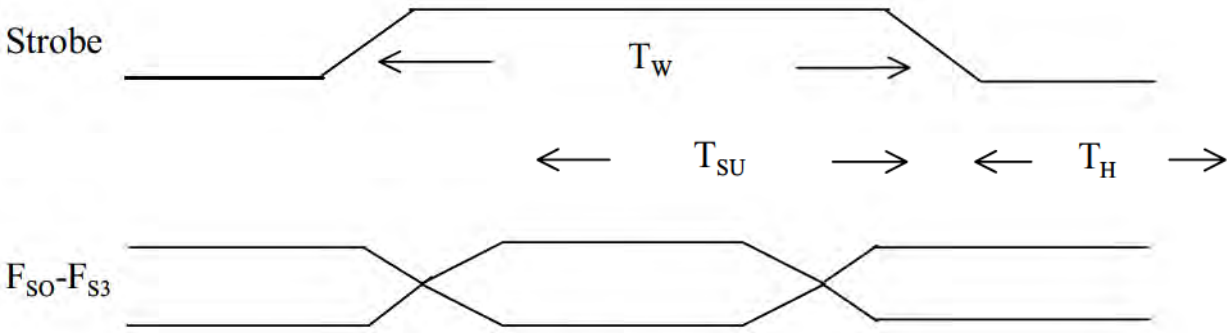
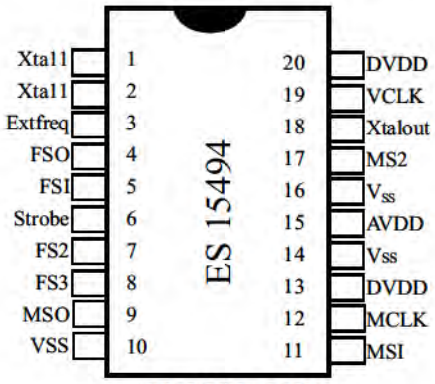


Figure 1. Timing diagram

PIN CONFIGURATION



20-PIN DIP
20-PIN SOP

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1.	Xta11	crystal oscillator input
2.	Xta12	crystal oscillator output
3.	Extfreq	external frequency input
4-5 7-8	F_{SO}, F_{S1} F_{S2}, F_{S3}	frequency select inputs for binary code corresponding to the video clock desired
6.	Strobe	strobe when high, allows new data into the frequency select latches
9, 11, 17	F_{S0} - F_{S2}	memory clock frequency select input
12.	MCLK	memory clock frequency output
12. 13. 14. 15. 16.	V_{SS} DV_{DD} V_{SS} AV_{DD} V_{SS}	ground digital power ground analog power ground All Vss pins must be connected
18.	Xtalout	crystal oscillator output buffer with a CMOS driver
19.	VCLK	Video clock frequency output
20.	DV_{DD}	Vidgital power

FUNCTION DESCRIPTION

The dual phase locked clock generator will derive its frequency from a crystal oscillator between pin1 and pin2(xtall and xta12). In addition to its internal generated clock. it can multiplex an external generated signal source to VCLK(pin 19)output via a mask option. The external signal input comes from Extfreq(pin 3). When it is selected, the PLL remains in lock at the preset value. It provides the ability to change frequencies rapidly. When this option is not selected by the ROM code. pin3 should be connected to Vss on PCB board.

Fs0-Fs3(pin 4, 5, 7, 8)are the video frequency select inputs corresponding to the frequency desired (see Table). As the pin6(Strobe)is high, it allows new data into the frequency select latches. Ms0-Ms2(pin 9, 11, 17)are the corresponding memory clock select inputs without strobe. 16 video clock frequencies and 8 memory clock frequencies are provided from the dual clock generator(see Table). If the pin 17 (Ms2)is grounded, we can get 4 memory clock frequencies from the generator. When floating, the input pins(pin 4, 5, 6, 7, 8, 9, 11, 17)are pulled high. A internal power-on reset signal will force the video clock select inputs to zero state to select a initial frequency.

BUFFERED XTALOUT

In some applications, it may be required to let the clock generator provide the bus clock for the rest of the system. This eliminates the need of an aditional 14.318MHz crystal oscillator in the system. To do this, the Xtalout(pin 18)output should be buffered with a CMOS driver

PCB LAYOUT CONSIDERATION

It is simple to utilize the ES15494 in VGA cards or on other motherboards, but does require to be careful in PC board layour. If the jitter-free performance must be satisfied, care should be taken in ensuring that the component not related to the ES15494 do not share the same ground. Multiple pins are utilized for all analog and digital V_{DD} and Vss connections to minimize the effect of packaging and the interaction of the digital and analog supply current. They also permit output frequency operation to exceed 140MHz. However, all V_{DD} and Vss pins must be connected.

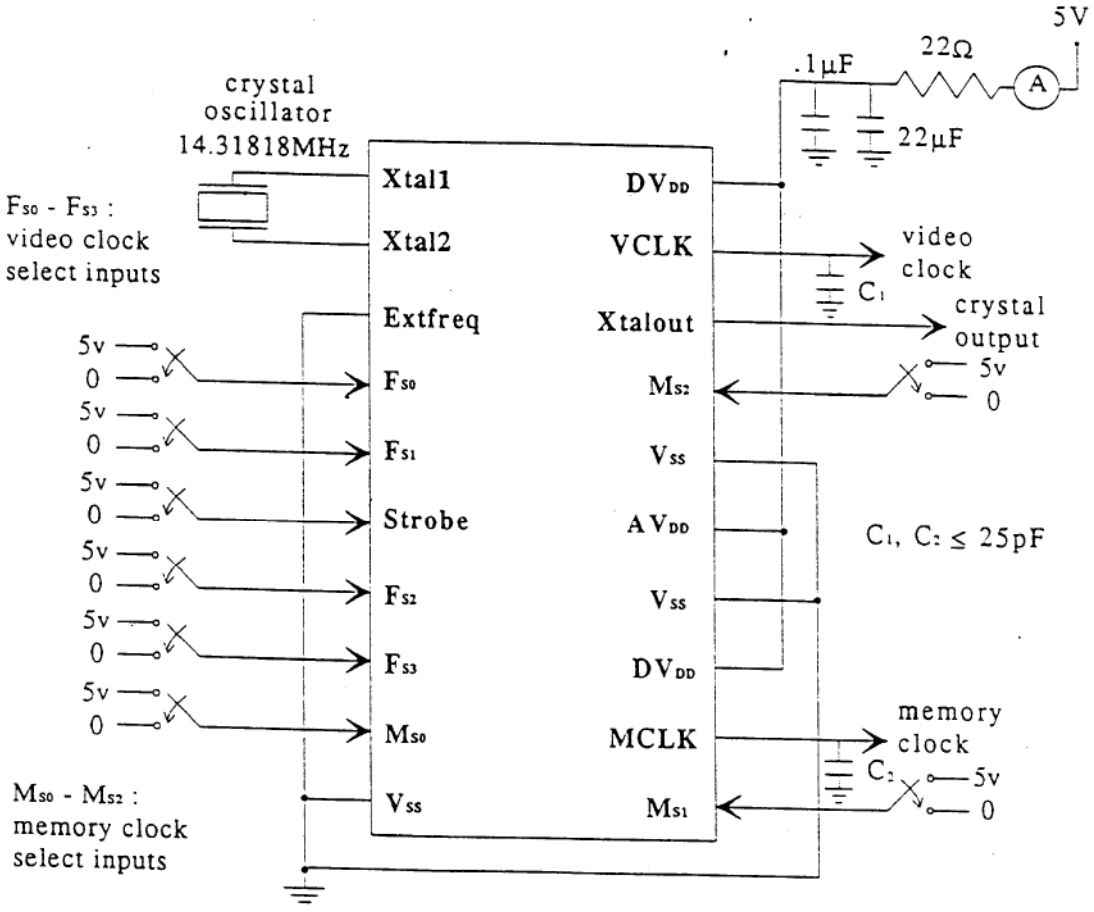


Figure 2. Test Circuit

(Test condition : C_{LOAD} = 25pF , T = 25 °C)